CONFIGURABLE SYNCHRONOUS OR ASYNCHRONOUS BUS INTERFACE

ABSTRACT OF THE DISCLOSURE

A system architecture and method allows for both synchronous and asynchronous communications on a common bus. Components that are able to reliably communicate via the bus using a synchronous interface are configured to communicate synchronously. Components that would require an unacceptable reduction in system-clock frequency to achieve synchronous communications are configured to communicate asynchronously. A bus controller facilitates bus arbitration, as well as synchronous-to-synchronous, synchronous-to-asynchronous and asynchronous-to-synchronous, and asynchronous-to-asynchronous transfers between components. To accommodate for physical layout dependencies, the components include a bus interface that is configurable for either synchronous or asynchronous communications, so that the determination of whether communications will be synchronous or asynchronous can be made after the layout is completed. The determination of whether a synchronous or asynchronous interface is used may also be dependent upon actual system performance, thereby facilitating a dynamic reconfiguration to optimize system performance.